

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of communicating between a media access control layer (MAC) and a physical layer (PHY), comprising:

receiving a first time-division multiplexed signal on a receive data pin;

receiving a plurality of time-division multiplexed receive control signals on a single receive control pin;

sending a second time-division multiplexed signal on a transmit data pin;

sending a plurality of time-division multiplexed transmit control signals on a single transmit control pin,

wherein the receive control signals include a receive data valid signal and a receive error signal time-division multiplexed together on the single receive control pin and the transmit control signals include a synchronization (SYNC) signal, a transmit enable signal and a transmit error signal time-division multiplexed together on the single transmit control pin,

2. (currently amended) The method of claim 1 wherein the time-division multiplexed receive control signals includes a plurality of 4 bit segments and wherein each 4 bit segment includes a synchronization bit.

3. (previously presented) The method of claim 2 wherein the beginning of each 4 bit segment of the receive control signals is determined by the synchronization bit of such each 4 bit segment.

4. (previously presented) The method of claim 1 wherein the time-division multiplexed receive control signals includes a plurality of 4 bit segments and wherein each 4 bit segment includes a receive data valid bit.

5. (previously presented) The method of claim 1 wherein the time-division multiplexed receive control signals includes 4 bit segments and wherein each 4 bit segment includes a receive error bit.

6. (previously presented) The method of claim 1 wherein the time-division multiplexed receive control signals includes a plurality of 4 bit segments and wherein each 4 bit segment includes a carrier sense bit.

7. (previously presented) The method of claim 1 wherein the time-division multiplexed transmit control signals includes a plurality of 4 bit segments and wherein each 4 bit segment includes a synchronization bit.

8. (previously presented) The method of claim 7 wherein the beginning of a each 4 bit segment is determined by the synchronization bit of such each 4 bit segment.

9. (previously presented) The method of claim 1 wherein the time-division multiplexed transmit control signals includes a plurality of 4 bit segments and wherein each 4 bit segment includes a transmit enable bit.

10. (previously presented) The method of claim 1 wherein the time-division multiplexed transmit control signals includes a plurality of 4 bit segments and wherein each 4 bit segment includes a transmit error bit.

11. (previously presented) The method of claim 1 further including indicating the speed of the PHY using the receive data pin.

12. (previously presented) The method of claim 11 wherein indicating the speed of the PHY using the receive data pin includes including an interface speed bit in a data segment when a receive control segment indicates no carrier sense, no receive data valid and no receive error.

13. (Original) The method of claim 1 further including buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long.

14. (Original) The method of claim 1 further including buffering data transmitted from the PHY to the MAC using an elasticity buffer that long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1%.

15. (Currently amended) An interface between a first media access control layer and a second media access control layer, ~~consisting essentially of~~ comprising:

a time-division multiplexed receive data pin;

a time-division multiplexed receive control pin for receiving different functional types of receive control signals including a receive data valid signal and a receive error signal that are time-division multiplexed together on the receive control pin;

a time-division multiplexed transmit data pin; and

a time-division multiplexed transmit control pin for transmitting different functional types of transmit control signals including a synchronization (SYNC) signal, a transmit enable

signal and a transmit error signal that are time-division multiplexed together on the transmit control pin.

16. (Currently amended) A media access control layer to physical layer interface ~~consisting essentially of~~ comprising:

a common clock;

a time-division multiplexed receive data pin;

a time-division multiplexed receive control pin for receiving different functional types of receive control signals including a receive data valid signal and a receive error signal time-division multiplexed together on the receive control pin;

a time-division multiplexed transmit data pin;

a time-division multiplexed transmit control pin for transmitting different functional types of transmit control signals including a synchronization (SYNC) signal, a transmit enable signal and a transmit error signal time-division multiplexed together on the transmit control pin.

17. (Previously presented) The interface of claim 16, wherein said time-division multiplexed receive control pin contains receive control signals further comprising a carrier sense signal and a synchronization (SYNC) signal.

18. (Canceled)

19. (previously presented) The method of claim 1, wherein the receive control signals further include a synchronization (SYNC) signal and a carrier sense signal.

20. (Cancelled)

21. (New) The interface of claim 15, wherein the receive control signals include a plurality of 4 bit segments and wherein each 4 bit segment includes a synchronization bit.

22. (New) The interface of claim 21 wherein the beginning of each 4 bit segment of the receive control signals is determined by the synchronization bit of such each 4 bit segment.

23. (New) The interface of claim 15 wherein the receive control signals include a plurality of 4 bit segments and wherein each 4 bit segment includes a receive data valid bit.

24. (New) The interface of claim 15 wherein the receive control signals includes 4 bit segments and wherein each 4 bit segment includes a receive error bit.

25. (New) The interface of claim 15 wherein the receive control signals includes a plurality of 4 bit segments and wherein each 4 bit segment includes a carrier sense bit.

26. (New) The interface of claim 15 wherein the transmit control signals includes a plurality of 4 bit segments and wherein each 4 bit segment includes a synchronization bit.

27. (New) The interface of claim 26 wherein the beginning of a each 4 bit segment is determined by the synchronization bit of such each 4 bit segment.

28. (New) The interface of claim 15 wherein the transmit control signals includes a plurality of 4 bit segments and wherein each 4 bit segment includes a transmit enable bit.

29. (New) The interface of claim 15 wherein the transmit control signals includes a plurality of 4 bit segments and wherein each 4 bit segment includes a transmit error bit.

30. (New) The interface of claim 15 wherein the receive data pin is further arranged to indicate the speed of the PHY.

31. (New) The interface of claim 30 wherein the receive data pin is arranged to indicate the speed of the PHY by including an interface speed bit in a data segment when a receive control segment indicates no carrier sense, no receive data valid and no receive error.

32. (New) The interface of claim 15 further comprising an elasticity buffer that is at least 27 bits long for buffering data transmitted from the PHY to the MAC.

33. (New) The interface of claim 15 further including an elasticity buffer that is long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1% and is arranged to buffer data transmitted from the PHY to the MAC.

34. (New) The interface of claim 15, wherein the receive control signals further include a synchronization (SYNC) signal and a carrier sense signal.

35. (New) An apparatus communicating between a media access control layer (MAC) and a physical layer (PHY), comprising:

means for receiving a first time-division multiplexed signal on a receive data pin;

means for receiving a plurality of time-division multiplexed receive control signals on a single receive control pin;

means for sending a second time-division multiplexed signal on a transmit data pin;

means for sending a plurality of time-division multiplexed transmit control signals on a single transmit control pin,

wherein the receive control signals include a receive data valid signal and a receive error signal time-division multiplexed together on the single receive control pin and the transmit control signals include a synchronization (SYNC) signal, a transmit enable signal and a transmit error signal time-division multiplexed together on the single transmit control pin.